

LISTING OF THE CLAIMS

1. (Previously Presented) A method of operating a pixel circuit, said method comprising:

accumulating photo-generated charge during an integration period;

turning on a transfer transistor to remove some of said accumulated photo-generated charge to a floating diffusion node;

turning on a reset transistor to remove said some of said accumulated photo-generated charge from said floating diffusion node; and

producing an output signal based at least in part on accumulated charges in the floating diffusion region existing at the end of said integration period.
2. (Original) A method as in claim 1, wherein said integration period includes a plurality of charge removal points.
3. (Original) A method as in claim 2, wherein said plurality of charge removal points each has an associated signal which controls the amount of accumulated photo-generated charges which are removed.
4. (Original) A method as in claim 3, wherein each said associated signals has a different signal characteristic from another associated signal such that different amounts of charges are removed by each of said associated signals.
5. (Original) A method as in claim 4, wherein said signal characteristic is a signal pulse amplitude.
6. (Original) A method as in claim 4, wherein said signal characteristic is a signal pulse width.
7. (Original) A method as in claim 4, wherein said signal characteristic is signal pulse width and signal pulse amplitude.

8. (Previously Presented) A method as in claim 1, wherein said photo-generated charges are accumulated by a photodiode.
9. (Original) A method as in claim 8, wherein said transfer transistor and reset transistor are turned on at the same time.
10. (Original) A method as in claim 8, wherein said reset transistor is turned on after said transfer transistor is turned on to remove charge from said photodiode to said floating diffusion node.
11. (Cancelled).
12. (Original) A method for operating a pixel circuit, said method comprising:
 - accumulating photo-generated charge in a photodiode during a charge integration period;
 - applying a first saturation control signal at a first voltage level to a transfer transistor during said integration period to remove some accumulated charge from said photodiode to a storage node;
 - applying a second saturation control signal to the transfer transistor during said integration period to remove additional accumulated charges from said photodiode; and
 - applying a reset pulse to a reset transistor coupled to said storage node each time a said first and second saturation control signal is applied.
13. (Original) The method of claim 12, wherein the second saturation control signal has a voltage that is smaller than the voltage of said first saturation control signal.
14. (Original) The method of claim 12, wherein said saturation control signals and reset signals are applied concurrently.

15. (Original) The method of claim 12, wherein said saturation control signals are respectively pulsed before the reset signals.
16. (Original) The method of claim 12, further comprising applying a third saturation control signal to said transfer transistor at the end of said integration period to transfer accumulated charges at said photodiode to a storage node.
17. (Original) The method of claim 16, wherein each of said first, second and third saturation control signals defines a segment of said integration period.
18. (Original) The method of claim 17, wherein the gain of each of the integration segments is different, and said gain of each integration portion is determined by the integration portion time period, and the voltage level of each respective saturation control signal.
19. (Original) A method for operating a pixel circuit, said method comprising the steps of:
 - accumulating photo-generated charge in a photodiode during a charge integration period;
 - applying a voltage at a transfer transistor in the pixel;
 - applying a first saturation control signal at a first voltage level to an anti-blooming transistor during said integration period to remove some accumulated charge from said photodiode to a storage node; and
 - applying a second saturation control signal to the anti-blooming transistor during said integration period to remove additional accumulated charges from said photodiode.
20. (Original) The method of claim 19, wherein the second saturation control signal has a voltage that is smaller than the voltage of said first saturation control signal.

21. (Original) The method of claim 20, further comprising applying a third saturation control signal to said transfer transistor at the end of said integration period to transfer accumulated charges at said photodiode to a storage node.
22. (Original) The method of claim 21, wherein each of said first, second and third saturation control signals defines a segment of said integration period.
23. (Original) The method of claim 22, wherein the gain of each of the integration segments is different, and said gain of each integration portion is determined by the integration portion time period, and the voltage level of each respective saturation control signal.
24. (Previously Presented) A method for operating a pixel circuit, said method comprising the steps of:

accumulating photo-generated charge in first and second photodiodes during a first and second charge integration period;

applying a first saturation control signal at a first voltage level to a first transfer transistor during said first integration period to remove some accumulated charge from said first photodiode to a storage node;

applying a second saturation control signal at a first voltage level to a second transfer transistor during said second integration period to remove some accumulated charge from said second photodiode to the storage node;

applying a third saturation control signal to the first transfer transistor during said first integration period to remove additional accumulated charges from said first photodiode;

applying a fourth saturation control signal to the second transfer transistor during said second integration period to remove additional accumulated charges from said second photodiode; and

applying a reset pulse to a reset transistor coupled to said storage node each time said first, second, third and fourth saturation control signal is applied.

25. (Original) The method of claim 24, wherein the third saturation control signal has a voltage that is smaller than the voltage of said first saturation control signal, and the fourth saturation control signal has a voltage that is smaller than the voltage of said second saturation control signal.
26. (Original) The method of claim 25, wherein said saturation control signals and reset signals are applied concurrently.
27. (Original) The method of claim 25, wherein said saturation control signals are respectively pulsed before the reset signals.
28. (Previously Presented) The method of claim 24, further comprising applying a fifth saturation control signal to said first transfer transistor at the end of said integration period to transfer accumulated charges at said first photodiode to the storage node, and a sixth saturation control signal to said second transfer transistor at the end of said integration period to transfer accumulated charges at said second photodiode to the storage node.
29. (Original) The method of claim 28, wherein each of said first, third and fifth saturation control signals defines a segment of said first integration period, and each of said second, fourth and sixth saturation control signals defines a segment of said second integration period.
30. (Original) The method of claim 29, wherein the gain of each of the integration segments is different, and said gain of each integration portion is determined by the integration portion time period, and the voltage level of each respective saturation control signal.

31. (Previously Presented) A pixel circuit, comprising:

a photocharge collection region;

a floating diffusion region, coupled to a reset node through a reset transistor; and

a transfer transistor, coupled between the photocharge collection region and said floating diffusion region,

wherein a signal controller is configured to apply a first saturation control signal at a first voltage level to said transfer transistor to start an integration period, to sequentially apply additional saturation control signals to the transfer transistor, each of said additional saturation control signals having voltage levels that are successively smaller than a prior saturation control signal, and to apply a reset pulse to a reset transistor each time additional saturation control signals are applied, wherein the signal controller is configured to apply said saturation control signals and reset signals simultaneously.

32. (Original) The pixel circuit of claim 31, wherein each application of an additional saturation control signal defines an integration portion in the integration period.

33. (Previously Presented) The pixel circuit of claim 32, wherein the additional saturation control signals comprise a second saturation control signal at a second voltage level that is lower than the first voltage level, said second saturation control signal defining a second integration portion in said integration period.

34. (Original) The pixel circuit of claim 33, the additional saturation control signals further comprise applying a third saturation control signal at a third voltage level that is lower than the second voltage level, said third saturation control signal defining a third integration portion in said integration period.

35. (Original) The pixel circuit of claim 34, wherein the additional saturation control signals further comprise applying a final saturation control signal at the first voltage level after the application of the third saturation control signal, said final saturation control signal ending the integration period.
36. (Original) The pixel circuit of claim 35, wherein the gain of each of the integration portions is different for the pixel circuit, said gain of each integration portion is determined by the integration portion time period, and the voltage level of each respective saturation control signal.
37. (Previously Presented) A pixel circuit, comprising:
- a photocharge collection region;
 - a floating diffusion region, said floating diffusion region being coupled to a reset node through a reset transistor, and further being coupled to said photocharge collection region through a transfer transistor;
 - an anti-blooming region for receiving charge from said photodiode collection region;
 - and
 - an anti-blooming transistor, said anti-blooming transistor configured to control the charge transferred from the photodiode collection region to the anti-blooming region,
- wherein a signal controller is configured to apply to said anti-blooming transistor a first saturation control signal at a first voltage level to start a first integration period, and to apply additional saturation control signals to the anti-blooming transistor, wherein each saturation control signal has a voltage level that is successively smaller with respect to a prior saturation control signal, and wherein each saturation control signal begins additional integration periods.

38. (Original) The pixel circuit of claim 37, wherein each application of an additional saturation control signal defines an integration portion in the integration period.
39. (Previously Presented) The pixel circuit of claim 38, wherein the signal controller is configured to apply a second saturation control signal at a second voltage level to the anti-blooming transistor that is lower than the first voltage level signal, said second saturation control signal defining a second integration portion in said integration period.
40. (Previously Presented) The pixel circuit of claim 39, wherein the signal controller is configured to apply a third saturation control signal at a third voltage level to the anti-blooming transistor that is lower than the second voltage level, said third saturation control signal defining a third integration portion in said integration period.
41. (Previously Presented) The pixel circuit of claim 40 wherein the signal controller is configured to apply a final saturation control signal at a full voltage level to the anti-blooming transistor after the application of the third saturation control signal, said final saturation control signal ending the integration period.
42. (Previously Presented) The pixel circuit of claim 41, wherein the gain of each of the integration portions is different, said gain of each integration portion being determined by the integration portion time period, and the voltage level of each respective saturation control signal.

43. (Previously Presented) A pixel circuit, comprising:

a first and second photocharge collection region;

a first floating diffusion region, coupled to a reset node through a reset transistor;

a second floating diffusion region, coupled to the first floating diffusion region;

a first transfer transistor, coupled between the first photocharge collection region and said first floating diffusion region; and

a second transfer transistor, coupled between the second photocharge collection region and said second floating diffusion region,

wherein a signal controller is configured to:

apply a first saturation control signal at a first voltage level to the first transistor to start a primary integration period, apply a plurality of successive saturation control signals to the first transfer transistor, each saturation control signal having a voltage level that is successively smaller with respect to a prior saturation control signal, each saturation control signal beginning additional integration periods;

apply a second saturation control signal at the first voltage level to the second transistor to start a secondary integration period, apply a plurality of successive saturation control signals are applied to the second transfer transistor, each saturation control signal having a voltage level that is successively smaller with respect to a prior saturation control signal, each saturation control signal beginning additional integration periods, said additional saturation control signals to the second transfer transistor not overlapping any of the additional saturation control signals to the first transfer transistor; and

apply the reset signal at the reset node concurrently with each application of the saturation control signal.

44. (Original) The pixel circuit of claim 43, wherein each application of an additional saturation control signal to the first transfer transistor defines an integration portion in the primary integration period.
45. (Previously Presented) The pixel circuit of claim 44, wherein the additional saturation control signals further comprise a second voltage level that is lower than the first voltage level, said second voltage level defining a second integration portion in said primary integration period.
46. (Previously Presented) The pixel circuit of claim 45, wherein the additional saturation control signals comprise a third voltage level that is lower than the second voltage level, said third voltage level defining a third integration portion in said primary integration period.
47. (Previously Presented) The pixel circuit of claim 46, wherein the additional saturation control signals comprise a final saturation control signal at the first voltage level after the application of the third voltage level, said final saturation control signal ending the integration period.
48. (Original) The pixel circuit of claim 47, wherein the gain of each of the integration portions is different, said gain of each integration portion is determined by the integration portion time period, and the voltage level of each respective saturation control signal.
49. (Original) The pixel circuit of claim 48, wherein each application of an additional saturation control signal to the second transfer transistor defines an integration portion in said secondary integration period.
50. (Previously Presented) The pixel circuit of claim 43, wherein the additional saturation control signals comprise a second saturation control signal at a voltage level that is lower than the first saturation control signal, said second saturation control signal defining a second integration portion in said secondary integration period.

51. (Previously Presented) The pixel circuit of claim 50, wherein the additional saturation control signals comprise a third saturation control signal at a voltage level that is lower than the second saturation control signal, said third saturation control signal defining a third integration portion in said secondary integration period.
52. (Previously Presented) The pixel circuit of claim 51, wherein the additional saturation control signals comprise a final saturation control signal at the first voltage level after the application of the third saturation control signal, said final saturation control signal ending the integration period.
53. (Original) The pixel circuit of claim 52, wherein the gain of each of the integration portions is different, said gain of each integration portion is determined by the integration portion time period, and the voltage level of each respective saturation control signal.